Parallel Resonance Type Fault Current Limiter

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***Abstract*—This paper proposes a new parallel LC resonance type fault current limiter (FCL) that uses a resistor in series with the capacitor. The proposed FCL is capable to limit fault current magnitude near to pre-fault magnitude of distribution feeder current by placing the mentioned resistor in the structure of FCL. In this way, voltage of point of common coupling (PCC) does not experience considerable sag during the fault. In addition, the proposed FCL does not use superconducting inductor which has high construction cost. Analytical analysis for this structure is presented in detail and simulation results using PSCAD/EMTDC software are obtained to validate the effectiveness of this structure. Also, an experimental setup is provided to show the accuracy of analytic analyses and simulation results.**

***Index Terms*—Parallel resonance, fault current limiter, resistor.**

I. Introduction

Growth of power systems and their interconnections has resulted in increasing the short circuit currents level. The most common ways to limit high-level fault currents are: upgrading switchgear and other equipments, splitting the power grid, using higher voltage connections (ac or dc), using high-impedance transformers and etc. These alternatives may create other problems such as loss of power system safety, reliability, high cost and more power losses [1-4].

Fault current limiters (FCLs) are developed to overcome above-mentioned problems. An ideal FCL should have the following characteristics [5, 6]:

a) Zero impedance in the normal operation;
b) No power loss in the normal operation;
c) Large impedance in the fault conditions;
d) Quick appearance of impedance when the fault occurs;
e) Fast recovery after fault removal.

The implementation of FCLs in electric power systems is not restricted to suppress the amplitudes of short circuit currents. They are also utilized to variety of performances such as power quality improvement, power system transient stability enhancement, reliability improvement and increasing transfer capacity of system electrical energy. Therefore, an ideal FCL should have another important characteristic in addition to listed characteristics. It should play the load impedance role and be equal to load impedance during fault to better operation in such performances [7-11].

Different topologies for the FCL are introduced in literatures such as superconducting FCLs (SFCLs), solid state FCLs, flux-lock type FCLs and resonance type SFCLs [12-19]. Resonance type FCLs limit the fault current by using various topologies of series or parallel LC resonant circuits [18-23]. Series resonance type FCLs are composed of series connection of a capacitor and a superconducting inductor. They do not allow the short circuit current to increase instantaneously as the fault occurs. However, these FCLs can not limit the fault current level, if the fault continues. So, the fault current will increase continually [18, 19]. Because of using superconducting inductor, some of these structures need high construction cost. So, they are not commercially available, especially for third world countries. On the other hand, resonance type FCLs which do not use superconducting inductor and replace it with an ordinary copper coil, make power losses in their structures [20- 21].

Previously introduced parallel resonance type FCLs have used two anti-parallel semiconductor switches to make resonance condition between L and C. Operation of such structures results in large oscillations on the line current caused by LC resonance at first moments of the fault. These oscillations may harm system equipments [22, 23].

In this paper, a new structure for parallel LC resonance type FCL is introduced. The proposed FCL uses a resistor in series with the capacitor and therefore it can simulate load impedance during fault. By this way, it can limit fault current level near to pre-fault condition. From power quality point of view, by equating fault current and before fault line current, the voltage of point of common coupling (PCC) will not experience considerable change during fault condition and power quality will improve. In comparison with the previously introduced resonance type FCLs, this FCL does not use the superconducting inductor in resonant circuit and as a result it is simpler to manufacture and has lower cost. Its inductor is bypassed, because of small voltage drop on the diode bridge in the normal operation and therefore, it has negligible power losses. On the other hand, by using the proposed FCL, the fault current will not increase continually, which happens in most of series resonance type FCLs. By using the resistor in this structure, problem of line current oscillations in the fault condition is solved. Analytical analysis and design

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considerations for this FCL are presented and MATLAB software [24] is used to solve the resulted formulas. The circuit operation in the normal and fault conditions are simulated by using PSCAD/EMTDC software [25]. Experimental results in laboratory scale are presented, too.

II. Power Circuit Topology and Principles of Operation

Fig. 1 shows single-phase power circuit topology of the proposed FCL. It is necessary to use a similar circuit for each phase in a three-phase distribution system. This structure is composed of two main parts which are as follows:

1) Bridge part: This part consists of a rectifier bridge containing D_1 to D_4 diodes, a small dc limiting reactor (L_{dc}), a self turn off semiconductor switch (such as *GTO*, *IGBT*, etc.) and its snubber circuit and a freewheeling diode (D_f).

2) Resonance part: This part consists of a parallel LC resonance circuit (L_{sh} and C_{sh}) (Its resonant frequency is equal to power system frequency) and a resistor in series with the capacitor, R_{sh}.

Bridge part of the proposed FCL operates as a high speed switch that changes fault current path to the resonance part, when the fault occurs. Obviously, it is possible to substitute this part with an anti-parallel connection of two self turn off semiconductor switches [22, 23]. Using a diode rectifier bridge has two advantages compared to two anti-parallel switches as follows:

1) This structure uses only one controllable semiconductor switch which operates in dc side instead of two switches that operate in ac side. The control circuit is simpler because of no need for ON/OFF switching in the normal operation case.

2) It is possible to use a small reactor in series with the semiconductor switch at dc side. This reactor plays two roles as follows:

(a) It is snubber for semiconductor switch;

(b) It is as a current limiter at first moments of fault occurrence.

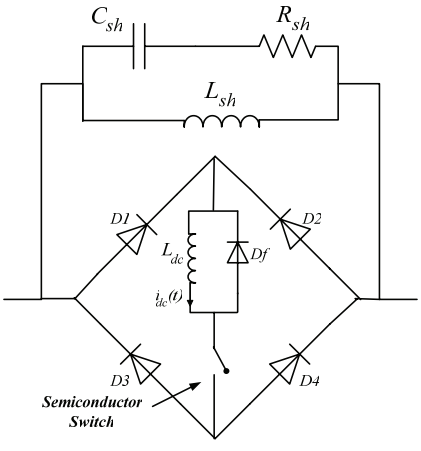

Figure 1. Single-phase power circuit topology of the proposed parallel resonance type FCL

However, placing dc reactor inside the bridge makes voltage drop on it because of dc current ripple. But, the current ripple is low and consequently voltage drop caused by it is not considerable in comparison with the feeder's voltage. Current ripple and voltage drop equations are studied completely in [6] and [26].

It is important to note that high rating semiconductor switches are commercially available with current rating up to 24kA and voltage rating up to 4kV [27]. Also, it is possible to use some series and/or parallel self turn off switches considering high current and voltage levels. The semiconductor switch needs suitable snubber circuit for its protection which is not shown in Fig. 1 for simplicity. Also, high rating semiconductor switches, their protection procedure and minimization of their power losses are discussed in [28-32].

From power loss point of view, in the normal condition, the proposed FCL has the losses on the rectifier bridge diodes, the semiconductor switch and small resistance of dc reactor. Each diode of the rectifier bridge is ON in half a cycle, while semiconductor switch is always ON. Therefore, the power losses of this FCL in the normal operation can be calculated as Eq. (1).

$$P_{loss} = P_R + P_D + P_{SW} = R_{dc} I_{dc}^2 + 4V_{DF} I_{ave.} + V_{SWF} I_{dc} \qquad (1)$$

where:

I_{dc} : dc side current which is equal to peak of line current (I_{peak});

R_{dc}: Resistance of dc reactor

V_{DF} : Forward voltage drop on each diode;

V_{SWF} : Forward voltage drop on the semiconductor switch;

$I_{ave.}$: Average of diodes current in each cycle that is equal to I_{peak} / π .

Considering Eq. (1) and the small value of dc reactor in this structure, total power losses of the proposed structure becomes a very small percentage of the feeder's transmitted power.

Fig. 2 shows the control circuit of the proposed FCL. In the normal operation of the power system, the semiconductor switch is ON. So, L_{dc} is charged to peak of the line current and behaves as a short circuit. Using semiconductor devices (diodes and semiconductor switch) and small dc reactor, cause a negligible voltage drop on the FCL.

When a fault occurs, dc current becomes greater than the maximum permissible current I_0 and the control circuit detects it and turns the semiconductor switch off. So, the bridge retreats from utility. At this moment, freewheeling diode D_f, turns on and provides free path for discharging the dc reactor. When the bridge turns off, fault current passes through the parallel resonance part of FCL. Consequently, large impedance enters to the circuit and prevents rising the fault current. In the fault condition, parallel LC circuit starts to resonance. In this case, because of resonance, the line current oscillates with large magnitude [22, 23]. These oscillations may lead to damage system equipments or put them in stress. But, by placing a resistor (R_{sh}) in series with the capacitor, current transients damp quickly that will be shown in simulations section. In addition, by using R_{sh}, voltage drop on R_{sh} leads to decrease voltage across the capacitor.

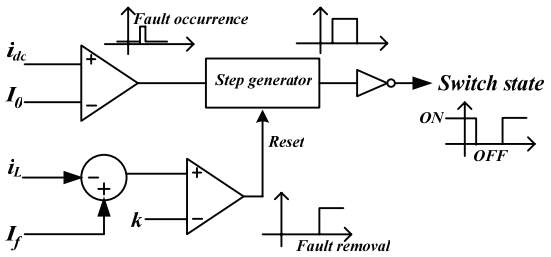

Figure 2. Control circuit of the proposed FCL

When the fault is disappeared, while semiconductor switch is OFF, parallel part of FCL will be connected in series with the load impedance. Therefore, line current will be decreased, instantaneously. To detect this instantaneous reduction of line current, i_L is compared with (I_f) that can be calculated from Eq. (2).

$$I_f = \frac{\left|\overline{V}_{PCC}\right|}{\left|Z_{eq}\right|} \tag{2}$$

where, Z_{eq} is the equivalent impedance of resonance part.

When the difference of i_L and I_f become greater than k as the fault removal sign, the control circuit turns the semiconductor switch ON. So, power system returns to the normal state. The value of k can be calculated from Eq. (3) as follow:

$$k = \frac{\left|\overline{V}_{PCC}\right|}{\left|\overline{Z}_{eq}\right|} - \frac{\left|\overline{V}_{PCC}\right|}{\left|\overline{Z}_{eq} + \overline{Z}_{L,\min}\right|} \tag{3}$$

where, $Z_{L,min}$ is the minimum impedance of load on the protected feeder.

As pointed, some of previously proposed FCL structures have ac power losses at resonant circuit in the normal condition, because of placing large inductor in the line current path [20, 21]. But, the proposed structure in this paper has very low losses in the normal condition, because the inductor is bypassed by the bridge part. Also, by choosing proper values for resonant circuit, the proposed FCL limits the fault current in a way that power system is not affected by the fault. In such condition, there will not be any considerable voltage sag on PCC voltage.

III. Analytical Analysis

Fig. 3 shows the single line diagram of power system including the proposed FCL. This figure is composed of power source, transformer, circuit breaker (C.B.), FCL, line impedance and load. The circuit breaker (C.B.) which is rated for the full system short circuit current is placed to ensure the adequate protection of power system during permanent faults. The utility voltage is a three-phase sinusoidal waveform. The utility side impedance is modeled by series connection of a resistor R_s and an inductor L_s.

Analytical analysis is discussed in two modes as follows:

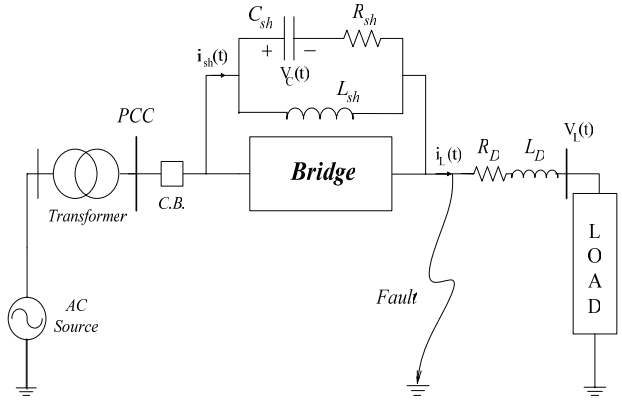

Figure 3. Single line diagram of power system

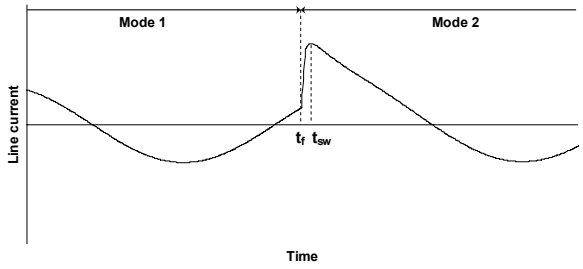

Figure 4. Enlarged view of line current before and after fault

Mode 1: Pre-fault steady state operation (until t_f in Fig. 4).

Mode 2: Between fault occurrence and fault removal (from t_f to fault removal time in Fig. 4).

A. Mode 1

In the normal operation of power system, the bridge part bypasses the resonant circuit. In this condition, the line current (i_L) can be expressed by differential equation (4):

$$V_s \sin(\omega t) = R i_L + \omega L \left(di_L / d\omega t\right) \tag{4}$$

where:

V_s : Peak of utility voltage

ω : Angular frequency of utility voltage

$R = R_s + R_L + R_D$ (Resistance of source side, load and distribution feeder, respectively)

$L = L_s + L_L + L_D$ (Inductance of source side, load and distribution feeder, respectively)

So, the line current equation can be derived as follow:

$$i_L(\omega t) = (V_s / \sqrt{R^2 + \omega^2 L^2})[(L\omega / \sqrt{R^2 + \omega^2 L^2}) e^{-(R/\omega L)\omega t} + \sin(\omega t - \varphi)] \tag{5}$$

where:

$$\varphi = \arctan(\omega L/R) \tag{6}$$

B. Mode 2

When a short circuit occurs, the dc limiting reactor can limit the increasing rate of fault current. The semiconductor switch doesn't operate until the line current reaches to a pre-defined value. By semiconductor switch operation in t_{sw} instant (Fig. 4), the bridge is switched off and the fault current is suppressed by resonant circuit. So, differential equation of fault current can be expressed as follow:

$$\begin{cases} L_s L_{sh} C_{sh} \left(d^3 i_L / dt^3\right) \\ +(R_s L_{sh} C_{sh} + L_s R_{sh} C_{sh} + R_{sh} L_{sh} C_{sh}) \left(d^2 i_L / dt^2\right) \\ +(L_s + R_{sh} C_{sh} R_s + L_{sh}) \left(di_L / dt\right) + R_s i_L = \\ (V_s - L_{sh} C_{sh} \omega^2) \sin(\omega t) + R_{sh} C_{sh} V_s \omega \cos(\omega t) \end{cases} \tag{7}$$

with initial values as follows:

$$\begin{cases} i_L(t = t_{sw}) = I_0 \\ \left(di_L/dt\right)(t = t_{sw}) = (V_s \sin(\omega t_{sw}) - I_0(R_s + R_{sh}))/L_s \\ \left(d^2 i_L/dt^2\right)(t = t_{sw}) = (V_s \omega \cos(\omega t_{sw}) \\ +I_0 \left(\left({R_{sh}}^2/L_{sh}\right) - \left(1/C_{sh}\right)\right) \\ -\left(\left((V_s \sin(\omega t_{sw}) - I_0(R_s + R_{sh}))\right)/L_s\right)(R_{sh} + R_s)) \end{cases} \tag{8}$$

where:

I_0 : Pre-defined line current for semiconductor switch operation.

Eq. (7) is solved by MATLAB software and its results are presented in simulations section in detail. After damping transients, the fault current equation can be expressed by Eq. (9).

$$i_L = A\cos(\omega t) + B\sin(\omega t) \tag{9}$$

where:

$$A = \frac{V_s\left[R_{sh}C_{sh}\omega(d' - b'\omega^2) - (1 - L_{sh}C_{sh}\omega^2)(c'\omega - a'\omega^3)\right]}{(c'\omega - a'\omega^3)^2 + (d' - b'\omega^2)^2}$$

$$B = \frac{V_s\left[R_{sh}C_{sh}\omega(a'\omega^3 - c'\omega) - (1 - L_{sh}C_{sh}\omega^2)(d' - b'\omega^2)\right]}{(c'\omega - a'\omega^3)^2 + (d' - b'\omega^2)^2}$$

$$a' = L_s L_{sh} C_{sh},$$

$$b' = R_s L_{sh} C_{sh} + L_s R_{sh} C_{sh} + R_{sh} L_{sh} C_{sh},$$

$$c' = L_s + R_{sh} C_{sh} R_s + L_{sh},$$

$$d' = R_s \tag{10}$$

By considering Eq. (9) and choosing proper values for L_{sh}, C_{sh} and R_{sh}, it is possible to limit the line current in the fault condition in a way that its value to be near to the pre-fault line current. In this case, if the fault occurs, PCC voltage will not sense the fault.

IV. Design Considerations

As discussed in section 2, L_{dc} is used to limit increasing speed of fault current and help the semiconductor switch to turn off in a safe condition. So, its value can be chosen by considering current characteristics of semiconductor switch.

For resonant circuit design, two main cases should be taken into account: first, equating resonance part equivalent impedance with load impedance; second, generated heat in resistor of resonance part during fault and its design problem. Equivalent impedance of resonance part, Z_{eq} can be derived as follow:

$$Z_{eq} = (R_{sh} - {j}/{\omega C_{sh}}) \| j\omega L_{sh} = {L_{sh}}/{C_{sh} R_{sh}} + j\omega L_{sh} \tag{11}$$

For equating this impedance with load impedance, L_{sh} should be equal to load inductance. Corresponding capacitor value, C_{sh} can be calculated considering resonance condition between it and L_{sh}. Finally, resistor value should be chosen in a way that $L_{sh}/C_{sh}R_{sh}$ be equal to load resistance. But, it is difficult to equate these impedances exactly and it is ideal case because of load variation on distribution feeders. From practical point of view, parameters of resonance part can be determined by using the history of measurements of load at protected feeder and discussed calculations.

Following discussion deals with the operation of the proposed structure in practical condition. Fig. 5 shows the magnitude of voltage deviation of PCC of test system from its base value (that is the pre-fault voltage magnitude of PCC). The horizontal axis of this figure shows the magnitude of impedance of load in per-unit where the base value is its impedance of ideal case. The dashed line shows the existence of ideal case. The parameter of this figure is the magnitude of source impedance. This figure shows that for a wide range of load magnitude variations (0.5 to 2 p.u. with fixed resonance part parameters), the voltage magnitude of PCC for post-fault condition changes in an acceptable range especially for low values of $|Z_s|$.

For considering the generated heat in resistance of resonance part, it is possible to change the values of L_{sh}, C_{sh} and R_{sh} and decrease the real part of Eq. (11). Note that the magnitude of Z_{eq} should be kept constant. Fig. 6 shows the fault current magnitude respect to R_{sh}. Parameter of this figure is resonant LC. Lower limit of R_{sh} is selected to ensure proper

transient response of resonant circuit. Standard values for C_{sh} are obtained from [33] and L_{sh} is calculated by considering resonance condition between it and C_{sh} in power frequency.

As a numerical example, it is considered that feeder's average current is 256A. In this condition, pre-desired value of fault current (256A) can be achieved by two values for resonant circuit parameters as follows:

Case 1: $C_{sh} = 150\mu F$, $L_{sh} = 68mH$, $R_{sh} = 16\Omega$
Case 2: $C_{sh} = 107\mu F$, $L_{sh} = 95mH$, $R_{sh} = 49\Omega$

$|Z_{eq}|$ in cases 1 and 2 are equal. However, in case (2), real part of Z_{eq} is smaller than its value in case (1). So, generated heat in R_{sh} is reduced in fault condition. As a result, design of R_{sh} becomes simpler from thermal point of view.

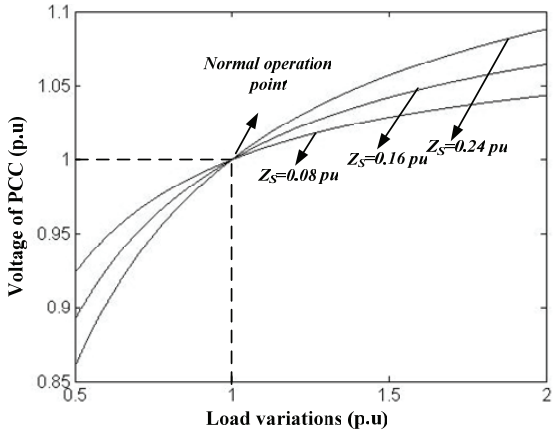

Figure 5. Voltage magnitude of PCC when equivalent impedance of resonance part is not equal to protected feeder load impedance (non-ideal case).

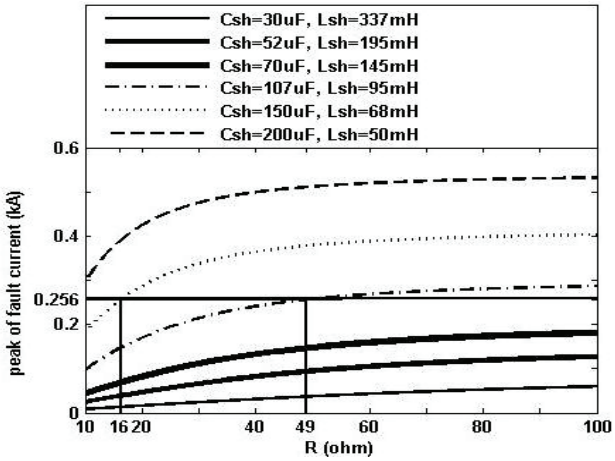

Figure 6. Variation of fault current magnitude respect to R_{sh}

V. Simulation Results

The power circuit topology of Fig. 3 is used for simulation in the fault condition. Simulation parameters are shown in Table I. Fault starts at 1s and continues to 1.12s (6 cycles of power frequency).

Simulation results for line current are shown in Fig. 7. Note that the current scales of figures are selected different to show more details. As fault occurs, without using FCL, fault current increases extremely and has asymmetrical nature (Fig. 7a). Also, without using R_{sh} in resonant circuit, transient oscillations appear on the line current caused by LC resonance as shown in Fig. 7b. After damping of these transients, line current becomes a small value near to zero. Fig. 7c shows the line current in the fault condition by using the proposed resonance type FCL. As shown in Fig. 7c, when fault current reaches to I_0 that is the pre-defined fault level, semiconductor switch turns off and line current is limited in the fault condition. After fault removal, the semiconductor switch turns on and line current returns to the normal state, after negligible distortion. Although the proposed FCL can limit the fault current, this current magnitude can vary according to Fig. 7c. Therefore, it is necessary to set the secondary switching device for full short circuit current of power system.

Fig. 8 shows dc reactor current. As the fault occurs, it starts to charge until semiconductor switch turning off. After semiconductor switch turning off, the freewheeling diode turns on and discharges L_{dc}. After fault removal, L_{dc} recharges because of resonant circuit voltage. By discharging resonant circuit, dc reactor current discharges and returns to the normal state.

Current of resonance part during the fault, $i_{sh}(t)$ for A phase is shown in Fig. 9. It is obvious that after semiconductor switch operation, line current will be equal to resonance part current. Fig. 10 shows the PCC voltage with and without using the proposed structure. As shown in this figure, the proposed FCL can prevent voltage sag on PCC, properly. Also, the PCC voltage without using R_{sh} in the proposed FCL is shown in Fig. 11.

It is observed that undesired distortions appear on the PCC voltage caused by the resonance current. The capacitor voltage is shown in Fig. 12.

TABLE I. Simulation System Parameters

Source Side Data	Power source	20 kV, 50Hz, $Z_{source} = 0.57 + j\omega 0.003\Omega$
	Transformer	20 kV/6.6 kV, 10 MVA, 0.1 p.u.
FCL Data	dc side	$L_{dc} = 0.01$ H, $V_{DF} = 3V, V_{SW} = 3V, I_0 = 0.5kA$
	Resonance part	$L_{sh} = 0.068$ H, $C_{sh} = 150\mu F$, $R_{sh} = 16\ \Omega$
Load Side Data	$Z_{line} = 0.5\Omega$, $Z_{load} = 15 + j\omega 0.1\Omega$	

To demonstrate the accuracy of calculations, differential equation (7) that shows the line current during fault, is solved by MATLAB software and its result is shown in Fig. 13. This figure is in good agreement with Fig. 7c. The peak value of current in both figures (Fig. 7c and 13) is 256A. Values and variation of curve show that results of calculations are adapted by simulation result of PSCAD/EMTDC software. This can prove the correction of Eq. (7) to (10).

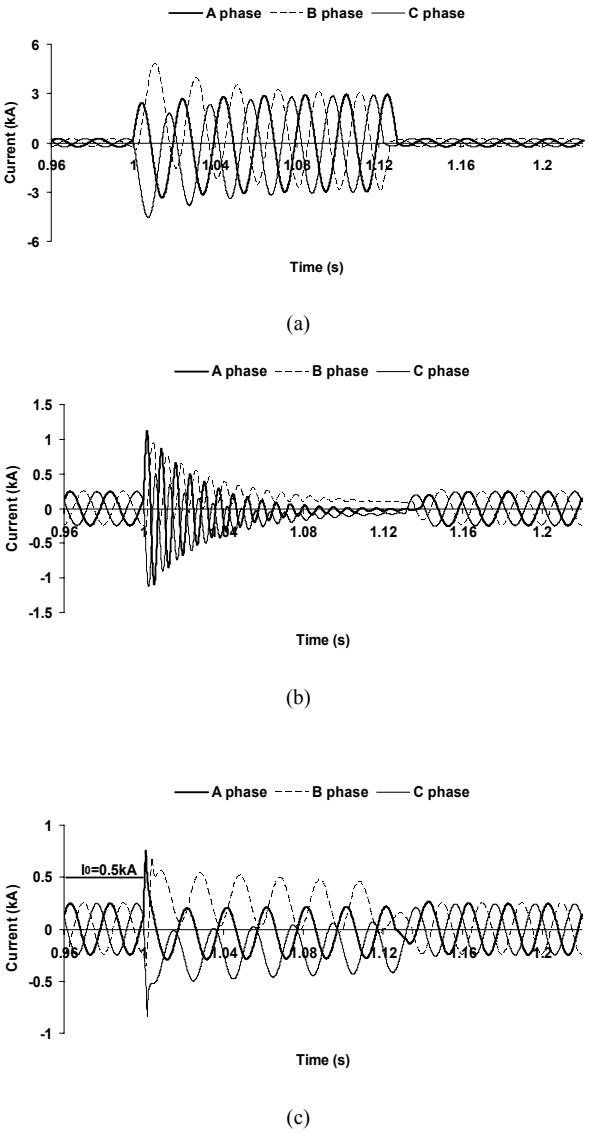

Figure 7. Fault current $i_L(t)$, (a) without FCL (b) without R_{sh} in resonance type FCL (c) with the proposed FCL

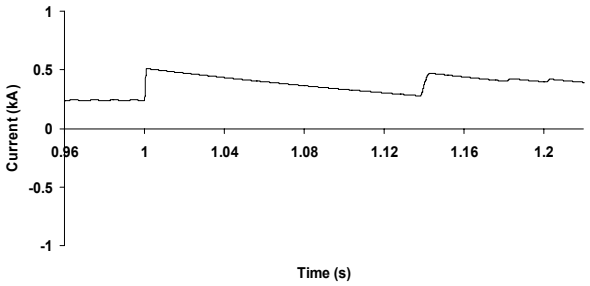

Figure 8. dc reactor current, $i_{dc}(t)$ for A phase

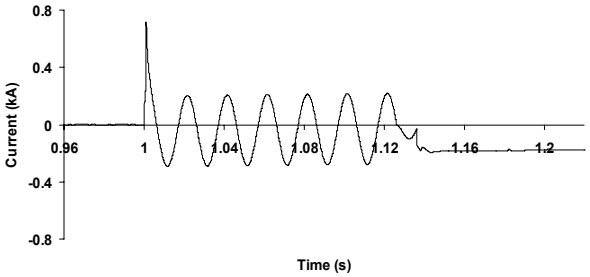

Figure 9. Resonance part current during the fault, $i_{sh}(t)$ for A phase

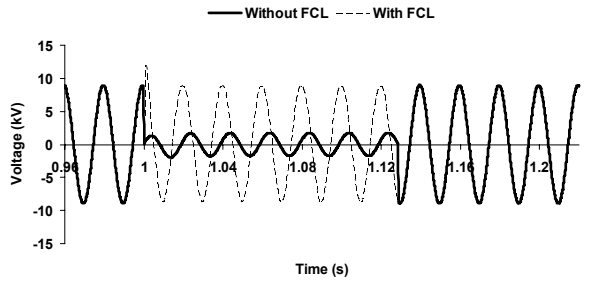

Figure 10. PCC voltage of A phase without (—) and with (----) the proposed FCL

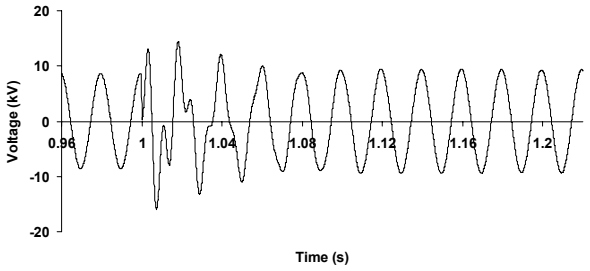

Figure 11. PCC voltage of A phase without using R_{sh} in the proposed FCL

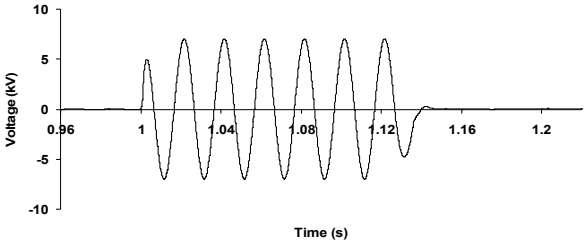

Figure 12. Capacitor voltage, $V_C(t)$ for A phase

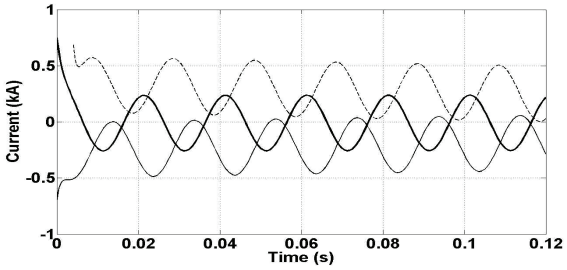

Figure 13. Calculated fault current, $i_L(t)$ by MATLAB software

To study the non-ideal case which is discussed in section 4, the load is changed to 0.5p.u. in simulation system and its results are presented in Figs. 14 and 15. Fig. 14 shows the line current (A phase) for non-ideal case. As shown in this figure, the line current is smaller than its value during fault. The PCC voltage in such condition is shown in Fig. 15. According to this figure, small voltage sag appears in PCC. This voltage sag is predictable considering Fig. 5 in the section 4.

To determine the rating of FCL components, it is possible to use simulation results as well as the design considerations mentioned in section 4. Of course, for all semiconductor devices, maximum on-state current is the peak of line current. The maximum off-state voltage for these devices is the PCC voltage during the fault. The current rating of L_{dc} is the peak of line current. Also, the resonance part inductance, L_{sh} will appear during the fault. Therefore, in the worst condition, its voltage will be PCC voltage. So, its current rating can be determined. For the capacitor C_{sh}, simple voltage dividing method can be used between it and the resistor R_{sh}.

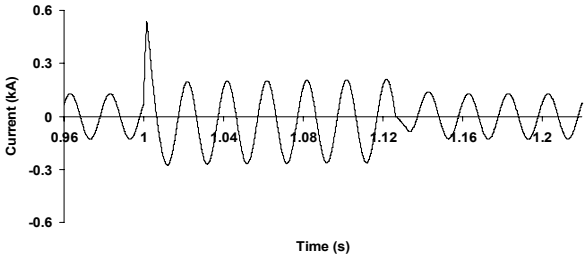

Figure 14. Line current of A phase in non-ideal case (A phase)

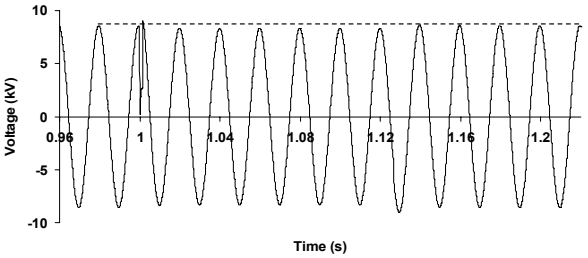

Figure 15. PCC voltage of A phase during the fault in non-ideal case

VI. Experimental Setup

The performance of proposed FCL is experimentally investigated using a laboratory scale power system simulator. The power system for experimental study is as Fig. 3. Note that the control circuit of the proposed FCL is implemented by software. Experimental setup parameters and control circuit data are presented in Table II. According to the available elements values in market and experimental setup facilities, the components values in experimental setup are selected as much as possible near to simulation values which were obtain by the proposed design procedure. Fig. 16 shows the line current by using the proposed FCL. This figure is in good agreement with Fig. 7c. Resonance part current during fault is shown in Fig. 17.

PCC voltage without using the proposed FCL is shown in Fig. 18. It is observed that PCC voltage drops strongly. Using the proposed FCL prevents this voltage sag as shown in Fig. 19. In such condition, a negligible distortion appears on PCC voltage at fault occurrence instant. Notice that the time scale in Fig. 19 is magnified to emphases on small distortion of voltage in fault instant. Fig. 18 and 19 are in accordance with Fig. 10. Fig. 20 shows the capacitor voltage in fault condition. It is in agreement with Fig. 12.

TABLE II. Experimental System Parameters

Source Side Data	Power source	220 V (peak), 50Hz, $Z_{source} = 0.5 + j\omega 0.005\Omega$
	Transformer	220 V/110V, 10 kVA, 0.1 p.u.
FCL Data	dc side	$L_{dc} = 0.01$ H, $V_{DF} = 1V, V_{SW} = 1V, I_0 = 8A$
	Resonance part	$L_{sh} = 0.07$ H, $C_{sh} = 150\mu F$ $R_{sh} = 15\ \Omega$
	Control circuit	Current sensor: CSNE151-100 Gate driver: IR2113 Microcontroller: ATMEGA32 Switch: GW40NC60V
Load Side Data	$Z_{line} = 0.5\Omega$, $Z_{load} = 10 + j25\Omega$	

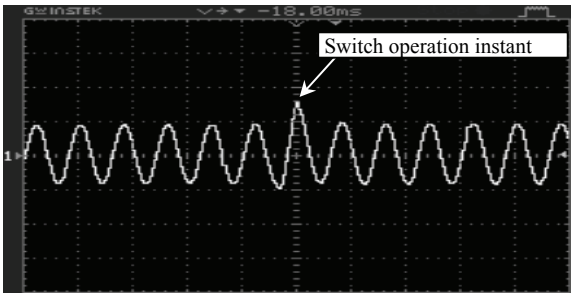

Figure 16. Line current by using the proposed FCL, (Amper/Div.: 5A, Time/Div. : 25 ms)

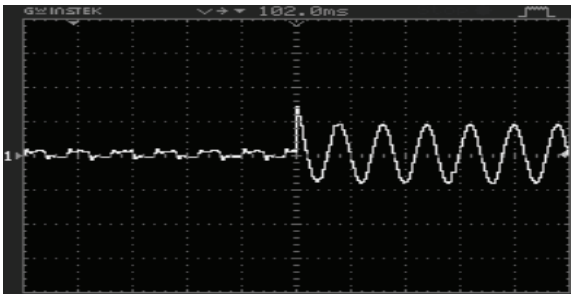

Figure 17. Current of resonance part during fault, (Amper/Div.: 5A, Time/Div.: 25 ms)

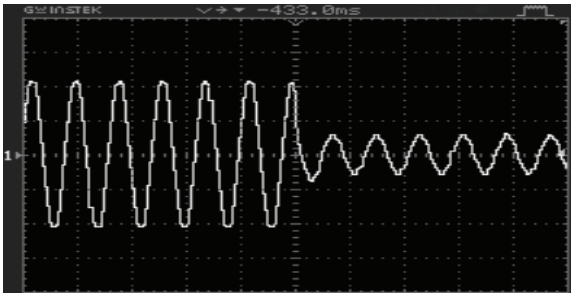

Figure 18. PCC voltage without using FCL, (Volt/Div.: 50V, Time/Div. 25 ms)

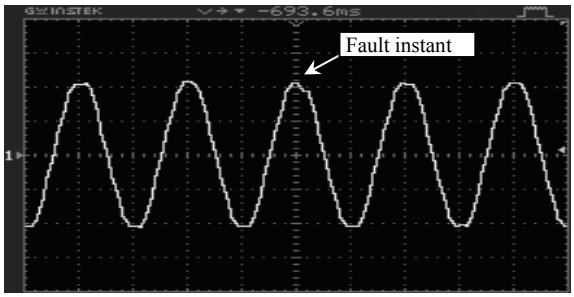

Figure 19. PCC voltage by proposed FCL, (Volt/Div.: 50V, Time/Div.: 10ms)

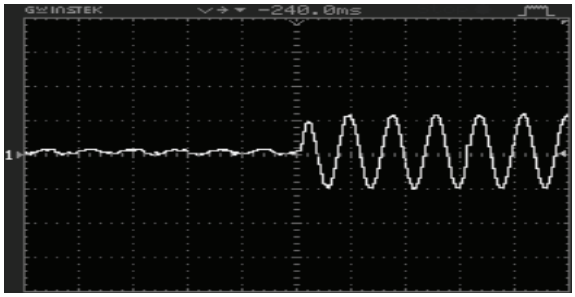

Figure 20. Capacitor voltage during fault, (Volt/Div.: 50V, Time/Div.: 25ms)

VII. CONCLUSION

In this paper, a new topology of parallel LC resonance type fault current limiter that includes a series resistor with the capacitor of LC circuit is introduced. The analytical analysis and design considerations for this structure are presented. The overall operation of mentioned FCL in normal and fault conditions are studied in detail. Also, simulation and experimental results are involved to validate analytic analyses. All early proposed FCLs have good current limiting characteristics. However, as shown in this paper, the proposed structure can improve power quality of distribution system in addition to fault current limiting. Proposed resonance type FCL can limit fault current in a way that PCC voltage does not face considerable sag during fault. This means that, in case of transient faults, it is not necessary to open the line by circuit breaker. By using R_{sh} in the proposed topology, transient state after fault damps quickly. In addition, it is capable of controlling fault current at constant value that is not possible in common series resonance type FCLs.

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